Scaling of Hydrogen-Terminated Diamond FETs to Sub-100-nm Gate Dimensions

David A. J. Moran, Oliver J. L. Fox, Helen McLelland, Stephen Russell, and Paul W. May

***Abstract*—We present the dc operation of hydrogen-terminated diamond field-effect transistors (FETs) with gate lengths of 1 μm to 50 nm. The 50-nm device metrics include a maximum drain current of 290 mA/mm and a peak extrinsic transconductance of 95 mS/mm. As the device gate length is reduced, peak intrinsic transconductance is increased substantially to a value of 650 mS/mm for the 50-nm device. A minimum $I_{\rm on}/I_{\rm off}$ ratio of $\sim$1.5 $\times$ 10^4 is maintained at this reduced gate dimension. These results appear highly promising for the improvement of hydrogen-terminated diamond FET high-frequency performance through reduction of the device gate length to sub-100-nm dimensions.**

***Index Terms*—Diamond, field-effect transistor (FET), hydrogen terminated, scaling.**

I. Introduction

MOTIVATED by the highly attractive intrinsic properties of the diamond material system [1], considerable effort has been focused on the development of hydrogen-terminated diamond field-effect transistors (FETs) as a high-power and high-frequency solid-state device solution. The high-frequency performance of diamond FETs has seen continuous improvement through the reduction of device gate length from the original demonstration of 2-μm gate length devices [2] to more recent gate dimensions of $\sim$ 100 nm [3]–[5]. To open up the microwave- and millimeter-wave frequency bands, however, further reduction in the gate length is required. To date, an investigation into the device operation and impact of short-channel effects for sub-100-nm devices has not been reported. Realization of the full potential of this technology therefore requires greater understanding of the impact of device scaling to these reduced dimensions. In this letter, we report on the dc operation and intrinsic scaling properties of 50-nm, 150-nm, 300-nm and 1-μm gate length devices.

II. Experiment

The material used for this study was CVD-grown 4.7 mm $\times$ 4.7 mm (001)-oriented single-crystal diamond from Element Six. Hydrogen termination of the sample was performed by exposing the diamond surface to H atoms created in a 1-kW microwave plasma. The process flow used for device realization is similar to that reported in [6] and is summarized as follows: Following hydrogenation, an 80-nm-thick Au metal layer was deposited to protect the diamond surface during device processing and to form the source and drain ohmic contacts as described hereinafter. Each of the subsequent lithographical stages was patterned using PMMA resist and a Vistec VB6 electron-beam lithography tool operating at 100 keV. Electrical isolation was achieved by exposure of the diamond surface to oxygen plasma after removal of the Au layer by KI wet etch. Gate lines of 50 nm, 150 nm, 300 nm, and 1 μm were written by electron-beam lithography at an exposure dose of 2000 μC/cm^2. Following development, the exposed Au layer was wet etched to form the ohmic contacts. A 25-nm Al/25-nm Au gate metal was then deposited through the same mask directly onto the exposed diamond. Substantial ohmic contact edge roughness results from this process (inset in Fig. 1) which is found to increase with reduced gate length. To enhance mechanical device yield, patterning and metallization of the 50-nm gate level was therefore performed as a separate level to that for the larger gate length devices to allow the use of a longer Au etch time during the source/drain contact formation phase.

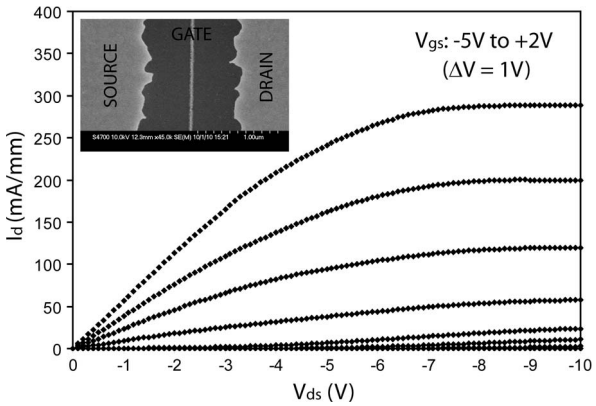

Fig. 1. DC output (I_d versus V_d with fixed $V_{\rm gs}$) characteristics and (inset) SEM image of a 50-nm gate length device demonstrating resultant ohmic contact edge roughness due to the gold etch.

III. Results and Discussion

The output characteristics of a typical 50-nm gate length device are shown in Fig. 1. Due to the observation of

Manuscript received January 13, 2011; revised February 7, 2011; accepted February 7, 2011. Date of publication March 21, 2011; date of current version April 27, 2011. This work was supported in part by the Engineering and Physical Sciences Research Council under Grant EP/E054668/1. The review of this letter was arranged by Editor C. Bulucea.

D. A. J. Moran, H. McLelland, and S. Russell are with the School of Engineering, University of Glasgow, G12 8LT Glasgow, U.K. (e-mail: david.moran@glasgow.ac.uk).

O. J. L. Fox and P. W. May are with the School of Chemistry, University of Bristol, BS8 1TS Bristol, U.K.

Digital Object Identifier 10.1109/LED.2011.2114871

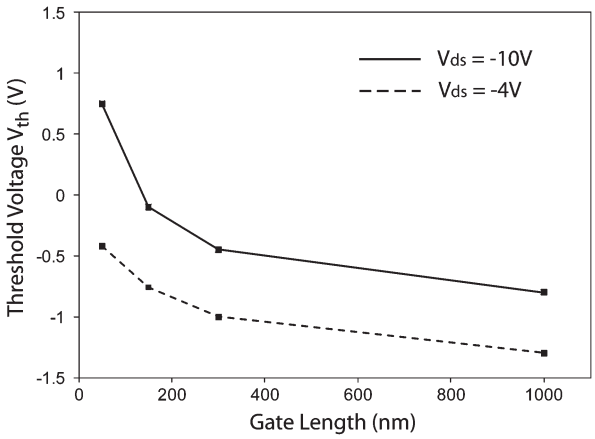

Fig. 2. Device $V_{\rm th}$ versus gate length for $V_{\rm ds} = -10$ V and $V_{\rm ds} = -4$ V. Although a positive shift in $V_{\rm th}$ is observed for both bias points as gate length is reduced, the rate of change in $V_{\rm th}$ is increased for $V_{\rm ds} = -10$ V in comparison with $V_{\rm ds} = -4$ V.

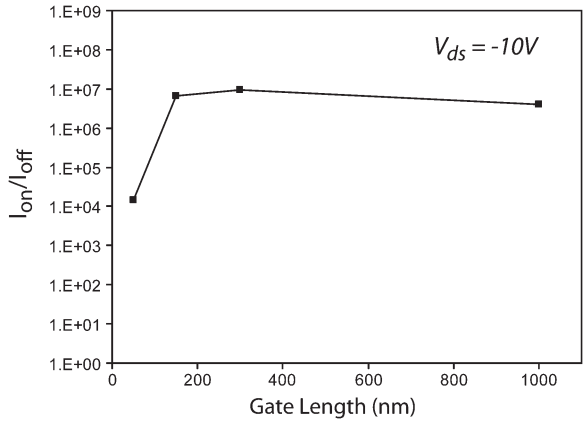

Fig. 3. Device $I_{\rm on}/I_{\rm off}$ versus gate length at $V_{\rm ds} = -10$ V. Little variation in $I_{\rm on}/I_{\rm off}$ occurs as gate length is reduced from 1 μm to 150 nm. Substantial reduction in $I_{\rm on}/I_{\rm off}$ occurs as gate length is reduced from 150 to 50 nm.

irreversible degradation to the device performance at a greater magnitude source/drain bias which can most likely be attributed to electrical instability of the hydrogen-terminated layer [1], the device operation is reported down to a minimum $V_{\rm ds}$ of -10 V. The maximum drain current $(I_{d\,\max})$ achieved was 380 $\pm$ 10 mA/mm for the 150- and 300-nm devices and 290 mA/mm for the 50-nm devices. This is comparable with that for single-crystal hydrogen-terminated diamond FETs described elsewhere [7]. An $I_{d\,\max}$ of 50 mA/mm was obtained for the 1-μm devices. Neither gate leakage current (typically on the order 1×10^{-5} I_d in this bias range) nor variation in access resistance can be attributed to this suppression of $I_{d\,\max}$ for the 1-μm device. The latter was determined by measurement of transmission line method (TLM) structures fabricated on the device sample which demonstrated a saturation current that is independent of a TLM ohmic contact separation of 450 mA/mm. A sheet resistance $R_{\rm sh}$ of 10 kΩ/sq and an ohmic contact resistance of 4.0 $\Omega \cdot$ mm were also extracted by TLM.

The threshold voltage $(V_{\rm th})$ (see Fig. 2) and $I_{\rm on}/I_{\rm off}$ (see Fig. 3) as functions of gate length were extracted from I_d–$V_{\rm gs}$ characteristics. Similar to that described for SiC FETs in [8], $V_{\rm th}$ is defined at a constant I_d which we take in this instance to be 1 mA/mm and at $V_{\rm ds} = -10$ V and $V_{\rm ds} = -4$ V. $I_{\rm on}/I_{\rm off}$ is defined as the ratio of the maximum I_d ($V_{\rm gs} = -5$ V) to the minimum I_d ($V_{\rm gs} = +2$ V) at the largest magnitude drain bias inspected of $V_{\rm ds} = -10$ V. As the gate length is reduced, $V_{\rm th}$ is found to shift more positively for both inspected drain bias points. This dimension-dependent variation in $V_{\rm th}$ becomes more pronounced as $V_{\rm ds}$ is reduced from -4 to -10 V due to a bias-associated increase in the OFF-state output conductance. A minimum $I_{\rm on}/I_{\rm off}$ of 1.5×10^4 however indicates that pinchoff of the drain current can still be maintained down to a gate length of 50 nm.

The dependence of the intrinsic transconductance $(g_m^{\rm int})$ with gate length was determined using the following expression [9]:

$$g_m^{\rm int} = \frac{g_m^{\rm ext}}{1 - R_s g_m^{\rm ext}} \tag{1}$$

where $g_m^{\rm ext}$ and R_s are the device-width normalized extrinsic transconductance and total source resistance, respectively. $g_m^{\rm ext}$ is measured directly, and R_s is defined as the sum of the source ohmic contact resistance $(R_{\rm cs})$ and the lateral access resistance through the diamond between the source and gate contacts $(R_{\rm ls})$. Given the substantial ohmic contact edge roughness (see Fig. 1), significant error in the calculation of $R_{\rm ls}$ can arise due to the inability to accurately determine the effective physical separation between source and gate contacts by visual inspection. Because of the nature of (1), such inaccuracy in the resultant value of R_s can lead to a large variation in the calculated value of $g_m^{\rm int}$. In this letter, R_s is instead extracted directly from the measured low-field axial resistance through each device $(R_{\rm on})$ at $V_{\rm ds} = -1$ V and $V_{\rm gs} = -5$ V. For this process, we assume the following: 1) the total source and drain resistances are equal due to the symmetric positioning of the ohmic contacts with respect to the gate and 2) the sheet resistance beneath the gate $(R_{\rm sh}^{\rm gate})$ when the transistor is fully on is comparable to the sheet resistance of the air-exposed device access regions as determined by TLM measurement $(R_{\rm sh}^{\rm TLM})$. $R_{\rm on}$ is then defined as

$$R_{\rm on} = 2R_s + R_{\rm sh}^{\rm gate} L_g \tag{2}$$

where each of the resistance terms in (2) is normalized to the width of the device. To account for the variation in $I_{d\,\max}$ of 290–380 mA/mm for device gate lengths of 50–300 nm, upper and lower values of 10 and 15 kΩ/sq for $R_{\rm sh}^{\rm gate}$ (based upon the TLM $I_{d\,\max}$ of 450 mA/mm and $R_{\rm sh}$ of 10 kΩ/sq) were considered for each gate length. The calculated peak $g_m^{\rm int}$ incorporating this variation in $R_{\rm sh}^{\rm gate}$ and the measured peak $g_m^{\rm ext}$ versus gate length are shown in Fig. 4. Data from the 1-μm devices are excluded in this analysis due to greater uncertainty in $R_{\rm sh}^{\rm gate}$, given the substantial reduction observed in $I_{d\,\max}$ (50 mA/mm) compared to that from TLM. Although $g_m^{\rm ext}$ is found to decrease slightly with gate length due to the process-related increase in source–gate contact separation and R_s as the gate length is reduced, $g_m^{\rm int}$ increases substantially across the inspected range of $R_{\rm sh}^{\rm gate}$. A peak $g_m^{\rm int}$ of 650 mS/mm is extracted for the 50-nm device. Assuming a constant gate

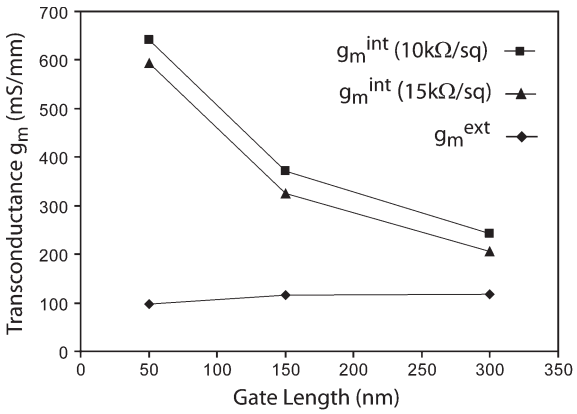

Fig. 4. Measured g_m^{ext} and extracted g_m^{int} for $R_{\mathrm{sh}}^{\mathrm{gate}}$ of 10 and 15 kΩ/sq versus device gate length. In contrast to the slight reduction of g_m^{ext} with gate length due to increased access resistance, g_m^{int} increases substantially as gate length is reduced for the inspected values of $R_{\mathrm{sh}}^{\mathrm{gate}}$.

capacitance per unit area (C_g) for each gate length, the velocity of charge beneath the gate contact (v_{car}) can be expressed as

$$v_{\mathrm{car}} = \frac{g_m^{\mathrm{int}}}{C_g}. \tag{3}$$

This suggests an increase in the intrinsic peak carrier velocity as the gate length is reduced and g_m^{int} is increased, perhaps leading to the measured reduction in $I_{d\max}$ for the 1-μm device. The variation in V_{th} and $I_{\mathrm{on}}/I_{\mathrm{off}}$ with reduced gate length further verifies the strong dependence of the intrinsic device operation upon the gate dimension within these devices.

IV. Summary

Hydrogen-terminated diamond FETs with a gate length from 1 μm to 50 nm have been fabricated, and their dc operation has been characterized. The 50-nm devices have demonstrated a maximum drain current of 290 mA/mm and a peak extrinsic transconductance of 95 mS/mm. Variations in the device threshold voltage and $I_{\mathrm{on}}/I_{\mathrm{off}}$ with gate length indicate the onset of short-channel effects as the gate length is reduced to 50 nm. However, a minimum $I_{\mathrm{on}}/I_{\mathrm{off}}$ of $\sim 1.5 \times 10^4$ is maintained for the 50-nm device across the inspected bias range. Furthermore, an increase in the device intrinsic transconductance is deduced as the gate length is minimized, with a peak value of 650 mS/mm extracted at a gate length of 50 nm. These results are encouraging for the potential improvement of hydrogen-terminated diamond FET high-frequency performance through scaling of the device gate length down to 50 nm.

Acknowledgment

The authors would like to thank Element Six Ltd. and Diamond Microwave Devices Ltd. for discussions and material supply and Prof. I. Thayne for useful discussions.

References

[1] A. Denisenko and E. Kohn, "Diamond power devices. Concepts and limits," *Diamond Relat. Mater.*, vol. 14, no. 3–7, pp. 491–498, Mar.–Jul. 2005.

[2] H. Taniuchi, H. Umezawa, T. Arima, M. Tachiki, and H. Kawarada, "High-frequency performance of diamond field-effect transistors," *IEEE Electron Device Lett.*, vol. 22, no. 8, pp. 390–392, Aug. 2001.

[3] K. Ueda, M. Kasu, Y. Yamauchi, T. Makimoto, M. Schwitters, D. J. Twitchen, G. A. Scarsbrook, and S. E. Coe, "Diamond FET using high-quality polycrystalline diamond with f_T of 45 GHz and $f_{\max}$ of 120 GHz," *IEEE Electron Device Lett.*, vol. 27, no. 7, pp. 570–572, Jul. 2006.

[4] A. Aleksov, A. Denisenko, U. Spitzberg, T. Jenkins, W. Ebert, and E. Kohn, "RF performance of surface channel diamond FETs with submicron gate length," *Diamond Relat. Mater.*, vol. 11, no. 3–6, pp. 382–386, Mar.–Jun. 2002.

[5] K. Hirama, H. Takayanagi, S. Yamauchi, Y. Jingu, H. Umezawa, and H. Kawarada, "High-performance p-channel diamond MOSFETs with alumina gate insulator," in *IEDM Tech. Dig.*, 2007, pp. 873–876.

[6] M. Kasu, K. Ueda, H. Kageshima, and Y. Yamauchi, "Gate interfacial layer in hydrogen-terminated diamond field-effect transistors," *Diamond Relat. Mater.*, vol. 17, no. 4/5, pp. 741–744, Apr./May 2008.

[7] M. Kasu, K. Ueda, H. Ye, Y. Yamauchi, S. Sasaki, and T. Makimoto, "2 W/mm output power density at 1 GHz for diamond FETs," *Electron. Lett.*, vol. 41, no. 22, pp. 1249–1250, Oct. 2005.

[8] T. Okayama, S. D. Arthur, J. L. Garrett, and M. V. Rao, "Bias-stress induced threshold voltage and drain current instability in 4H–SiC DMOSFETs," *Solid State Electron.*, vol. 52, no. 1, pp. 164–170, Jan. 2008.

[9] H. Matsudaira, S. Miyamoto, H. Ishizaka, H. Umezawa, and H. Kawarada, "Over 20 GHz cut-off frequency deep sub-micron gate diamond MISFET," *IEEE Electron Device Lett.*, vol. 25, no. 7, pp. 480–482, Jul. 2004.